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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/506,322	09/02/2004	Hiroshi Iwata	0020-5289PUS1	8818

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EXAMINER	
HOANG, HUAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/506,322	IWATA ET AL.	
	Examiner	Art Unit	
	Huan Hoang	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☒ Claim(s) *6 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *090204 & 070805*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims "1, 2, 8", "9" and "10" are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims "1", "9" and "10", respectively, of copending Application No. 10/505,433 in view of Yoshikawa (US Patent No. 6,335,554 cited by Applicant).

Claims differ from claims of the copending Application No.10/505,433 in reciting the voltages applied to the gate, the source and drain to perform memory operations. However, Yoshikawa discloses the voltages applied to the gate, the source and the drain to change the current amount between the source and drain by an amount of

electric charges in the charge holding portions (column 7, lines 11-16) and a second voltage (-6V) applied to the gate electrode such that carriers are injected into the charge holding portion existing on the side of one of the second conductivity diffusion layer regions. It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply the voltages of Yoshikawa to the gate, the source and the drain to perform memory programming and erasing operations.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 and 8-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa (US Patent No. 6,335,554 cited by Applicant).

Yoshikawa discloses a semiconductor storage device having all the elements as recited in claims1-5 and 8-15 as follows:

a first conductivity type semiconductor substrate (1, Fig. 1);

a gate insulating film (2, Fig. 1);

a single gate electrode(3, Fig. 1) formed on the gate insulating film;

two charge holding portions (4a and 4b, Fig. 1) formed on sides of side walls of the single electrode;

a channel region disposed under the single gate electrode; and

second conductivity type diffusion (n+ and n-) layer regions disposed on both sides of the channel region, wherein the charge holding are structured so as to change a current amount flowing between one of the second conductivity type diffusion layer regions and the other of the second conductivity type diffusion layer regions when voltage (10V, Fig. 2A) is applied to the gate electrode by an amount of electric charges stored in the charge holding portions (column 7, lines 11-16), wherein a reference voltage (0v) is applied to the other of the second conductivity type diffusion layer regions, a first voltage (8V) is applied to the one of the second conductivity type diffusion layer regions, and a second voltage (-6V) is applied to the gate electrode such that carriers are injected into the charge holding portion existing on the side of one of the second conductivity diffusion layer regions, wherein a third voltage (column 10, lines 35-37) is applied to the first conductivity type semiconductor substrate; wherein the first conductivity is P-type (column 6, line 40), wherein the first conductivity type is N type (Fig. 7), the carriers are positive holes (holes and electrons move in opposite directions), the first voltage (8V) is higher than the reference voltage (0V) and the second voltage (-6V) is lower than the reference voltage (0V), wherein the charge holding portion is composed of a first insulator, a second insulator and a third insulator (column 6, lines 31-33); wherein a thickness of the film (10nm, oxide film 5) composed of the second insulator on the channel region is smaller than the gate insulating film (25 nm, gate insulation film 2) and is 0.8nm or more, wherein a thickness of the film composed of the second insulator on the channel is larger than a thickness of the gate

insulating film (4nm, column 24, lines 62-64), wherein the film composed of the first insulator includes a portion having a surface that is approximately parallel to the surface of the gate insulating film and a portion extending in direction approximately parallel to a lateral side of the gate electrode (Fig. 1), wherein at least part of the charge holding portion is formed so as to overlap part of the second conductivity type diffusion layer region (Fig. 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa.

Yoshikawa discloses all the limitations of claim 7 except for the gate length of the gate electrode being between 0.015 μm and 0.5 μm. However, Fujiwara discloses the use of the gate length of 90 nm to reduce the threshold voltage (paragraph **[0140]**). It would have been obvious to one having ordinary skill in the art at the time the invention was made to us the gate length of 90 nm in order to reduce the threshold voltage.

Allowable Subject Matter

7. Claims 6 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or suggest the following:

"wherein an absolute value of voltage difference between the second voltage and the third voltage is 0.7V or more and 1V or less." as recited in claims 6 and 16.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huan Hoang whose telephone number is (571) 272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Huan Hoang
Primary Examiner
Art Unit 2827

HH
4/15/06